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[c1] A method of forming a device including a conductor and a contact over a semiconductor substrate comprising the steps as follows:
depositing a first dielectric layer on a semiconductor substrate with a top surface;
depositing a first hard mask layer over the top surface of the first dielectric layer;
forming a conductor line slot in the device extending through the hard mask and at least down into the first dielectric layer;

forming a conductor in the conductor line slot below the top surface of the first hard mask layer;
widening the conductor line slot in the hard mask layer to form a widened conductor line slot;
forming a capping layer in the widened conductor line slot covering the conductor;
depositing a second dielectric layer over the device;
etching an initial contact hole through the second dielectric layer down to the top surface of the first hard mask layer;

etching a deep contact hole through first hard mask layer and first dielectric layer down to the substrate with

an etchant selective to the capping layer; and
filling the deep contact hole and the initial contact hole with contact metallization.

[c2] The method of claim 1 wherein the conductor line slot in the device extends through the hard mask and through the first dielectric layer and down to the substrate.

[c3] The method of claim 2 wherein a dielectric layer is formed on the surface of the substrate after forming the conductor line slot down to the substrate and before forming the conductor in the conductor slot.

[c4] The method of claim 1 wherein the etching of the deep contact hole forms a smooth tapered spacer surface in the deep contact hole on the capping layer over the conductor.

[c5] The method of claim 1 wherein the conductor line slot in the device extends through the hard mask and through only a portion of the first dielectric layer to a depth above the substrate.

[c6] The method of claim 1 wherein the first dielectric layer comprises a low k dielectric material and the capping layer comprises silicon nitride.

[c7] The method of claim 1 wherein the first dielectric layer

comprises High Density Plasma (HDP) silicon oxide and the capping layer comprises silicon nitride.

[c8] The method of claim 1 wherein a second hard mask layer and a patterned photoresist mask are formed over the second dielectric layer before etching the contact hole through the second dielectric layer down to the top surface of the first hard mask layer and the patterned photoresist mask and the second hard mask layer are employed for patterning the initial contact hole.

[c9] The method of claim 1 wherein the conductor comprises a damascene conductor formed from conformal underlayers etched back into the slot.

[c10] The method of claim 1 wherein the conductor comprises a silicide conductor.

[c11] A method of forming a device including a conductor and a Self-Aligned Contact (SAC) over a semiconductor substrate comprising the steps as follows:
depositing a first InterLayer Dielectric (ILD1) layer on a semiconductor substrate with a top surface;
depositing a first hard mask layer (HM1) having a top surface over the top surface of the ILD1 layer;
forming a conductor line slot in the device extending through the hard mask and at least down into the ILD1 layer;
forming a conductor in the conductor line slot below the top surface of the HM1 layer;
widening the conductor line slot in the HM1 layer to form a widened conductor liner slot above the ILD1 layer;
forming a capping layer composed of silicon nitride in the widened conductor line slot covering the conductor and overhanging the ILD1 layer;
planarizing the capping layer to the top surface of the HM1 layer;

depositing a second first InterLayer Dielectric (ILD2) layer over the device;

forming a second hard mask layer (HM2) over the ILD2 layer;

forming a photoresist mask over the HM2 layer;

etching an initial contact hole through the photoresist mask, the HM2 layer and the second dielectric layer down to the top surface of the HM1 layer;

etching a deep contact hole through the HM1 layer and ILD1 layer down to the substrate with an etchant selective to the capping layer; and

filling the deep contact hole and the initial contact hole with contact metallization.

[c12] The method of claim 11 wherein the conductor line slot in the device extends through the HM1 mask and

through the ILD1 layer and down to the substrate.

[c13] The method of claim 12 wherein a dielectric layer is formed on the surface of the substrate after forming the conductor line slot down to the substrate and before forming the conductor in the conductor slot.

[c14] The method of claim 11 wherein the etching of the deep contact hole forms a smooth tapered spacer surface in the deep contact hole on the capping layer over the conductor.

[c15] The method of claim 11 wherein the conductor line slot in the device extends through the HM1 mask and through only a portion of the ILD1 layer to a depth above the substrate.

[c16] The method of claim 11 wherein the ILD1 layer comprises a low k dielectric material.

[c17] The method of claim 11 wherein the ILD1 layer comprises High Density Plasma (HDP) silicon oxide.

[c18] The method of claim 11 wherein the conductor comprises a damascene conductor formed from conformal underlayers etched back into the slot.

[c19] The method of claim 11 wherein the conductor comprises a silicide conductor.

CLAIM 20. (CANCELLED)